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Fast floating-point normalisation unit realised using NOR planes

Kyung-Nam Han, Sang-Wook Han and Euisik Yoon

A new floating-point (FP) normalisation unit scheme is presented, that achieves enhanced performance by merging a leading zero counter (LZC) and a normalisation shifter. The LZC and the shift decoder are combined by using NOR planes to generate control signals directly to the normalisation shifter. The chip has been fabricated with a five-metal 0.18 μm CMOS process and performs the 64 bit FP normalisation within 1.4 ns.

Introduction: When floating-point (FP) addition or subtraction occurs, a normalisation process is inevitably required to get the IEEE 754 standard number. The procedure of normalisation is: (i) to count the leading zeros from the addition/subtraction result; and (ii) to shift the result according to the counted number. Therefore, a special counter block known as a leading-zero counter (LZC) and a left shifter called a normalisation shifter are required. The main purpose of the LZC block is to give the shift amount value to the normalisation shifter. However, the LZC block is usually as slow as a significand adder because it eventually has a carry-propagating operation. To improve the performance, the LZC has been implemented in logarithmic structures using binary or trinary trees [1–3].

In this Letter, a new method of FP normalisation is presented. The conventional approach that uses the LZC result is significantly modified in the proposed structure. An OR-AND plane, which can be implemented with NOR planes, finds the shift amount value. It generates a leading one's position value (LOPV) instead of the shift amount value. The LOPV can be generated faster than the conventional shift amount value and the LOPV can also be directly decoded to control the shift mux by an additional NOR plane. The proposed normalisation scheme is fabricated using a 0.18 μm CMOS technology. The measured result shows a delay time of 1.4 ns under the condition of 1.8 V supply voltage.

Proposed normalisation scheme: A typical conventional normalisation method is to shift the operand after the LZC calculates the shift amount value, which is a 6-bit number for a 64-bit operand. However, the LZC is typically a complicated block that introduces a long delay time to produce a shift amount value; hence, a leading zero anticipatory (LZA) logic has been an alternative approach to conceal the delay of the LZC block behind the significand adder [3]. In our proposed scheme, instead of using the LZC to get a 6-bit shift amount value, an OR-AND plane has been devised to produce an LOPV that will be directly decoded for the shifter, as shown in Fig. 1. This OR-AND plane can be implemented in a simpler and faster structure than the conventional LZCs. The LOPV is the number that every bit is forced to be zero except for the leading one bit of the input operand. For example, if an 8-bit input operand is 00001011, then the LOPV will be 00001000. The OR-AND plane can be practically implemented using a NOR-NOR plane, like a programmable logic array (PLA) structure. From this number, both the shift control signals and the conventional shift amount value for the exponent calculation are acquired by simple additional OR operations. Described below is the procedure for generating the LOPV.

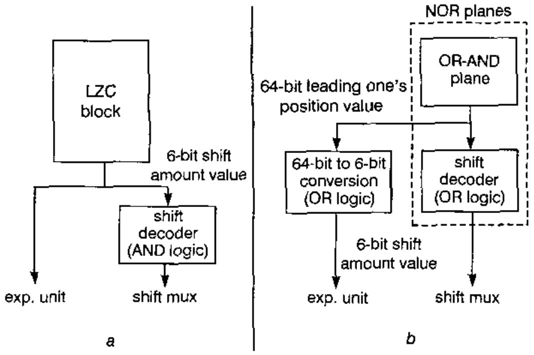

Fig. 1 *Comparison between conventional and proposed normalisation method*

a Conventional
b Proposed

Let A be an input operand of the n-bit FP normalisation unit and $A \neq 0$. Then,

$$A = \sum_{i=0}^{n-1} a_i 2^i = \sum_{i=M+1}^{n-1} 0 \cdot 2^i + a_M 2^M + \sum_{i=0}^{M-1} a_i 2^i \tag{1}$$

where M is a leading one's position and $a_i = 0$ for $M+1 \leq a_i \leq n-1$. The number LOPV of A is the number that all a_i become zero except for the leading one bit, a_M; therefore, given by $LOPV = a_M 2^M$. The shift control signals are generated from the LOPV, not from the conventional shift amount value which is $n-M-1$. From the LOPV, the shift control signals are produced through simple OR operations. Let us now define some basic bit-operators for the simple description of equations:

$$\bigcup_{i=0}^{n-1} a_i \equiv a_0 \vee a_1 \vee \cdots \vee a_{n-1} \tag{2}$$

$$\prod_{i=0}^{n-1} a_i \equiv a_0 \times a_1 \times \cdots \times a_{n-1} = a_0 \wedge a_1 \wedge \cdots \wedge a_{n-1} \tag{3}$$

Here, (2) represents the existence of the '1' inside the region of $0 \leq i \leq n-1$. Let us now check the leading one at the upper half region. An operation, $\bigcup_{i=n/2}^{n-1} a_i$, indicates that if the result is '1', then the leading one value is in the upper half region, and that if not, then in the lower half region. Let B_1 be the result of the half region check, so that

$$B_1 = \sum_{i=0}^{n-1} b_{1,i} 2^i = \begin{cases} \bigcup_{i=n/2}^{n-1} a_i & \text{if } \frac{n}{2} \leq i \leq n-1 \\ \overline{\bigcup_{i=n/2}^{n-1} a_i} & \text{if } 0 \leq i \leq \frac{n}{2} - 1 \end{cases} \tag{4}$$

In (4), the bar notation means the inversion operation. Next, the leading one check region is further subdivided into four regions in order to narrow down the possible leading one region in the next half segments. Let B_2 be the result of the quarter region check, so that

$$B_2 = \sum_{i=0}^{n-1} b_{2,i}2^i = \begin{cases} \bigcup_{i=3n/4}^{n-1} a_i & \text{if } \frac{3n}{4} \le i \le n-1 \\ \overline{\bigcup_{i=3n/4}^{n-1} a_i} & \text{if } \frac{n}{2} \le i \le \frac{3n}{4}-1 \\ \bigcup_{i=n/4}^{(n/2)-1} a_i & \text{if } \frac{n}{4} \le i \le \frac{n}{2}-1 \\ \overline{\bigcup_{i=n/4}^{(n/2)-1} a_i} & \text{if } 0 \le i \le \frac{n}{4}-1 \end{cases} \quad (5)$$

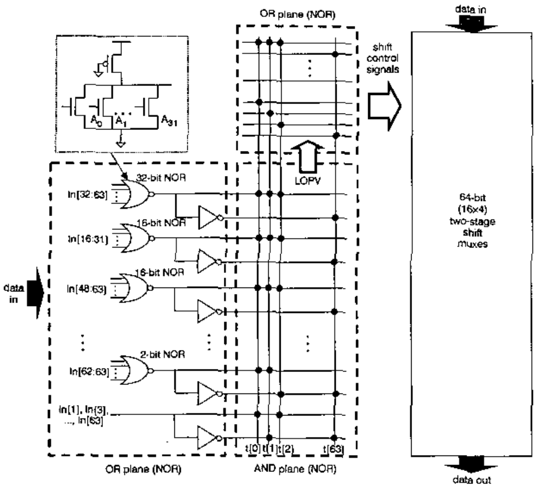

Fig. 2 *Circuit diagram of proposed normalisation scheme*

With a bit by bit AND operation from B_1 and B_2 results, $B_1 \wedge B_2$, only the quarter region that includes the leading one becomes '1' and other regions are set to zero. Now, the region of the leading one check is more fractionised, so that B_3 is subdivided into eight segments and B_4 into 16 segments until no more subdivision is possible. This is the logarithmic subdivision and $\log_2 n$ leading one check is required to get the LOPV for the n-bit input operand. The LOPV acquired can be expressed in (6):

$$LOPV = \sum_{i=0}^{n-1} c_i 2^i = B_1 \wedge B_2 \wedge \cdots \wedge B_{\log_2 n} = a_M 2^M \quad (6)$$

where $c_i = \prod_{k=0}^{\log_2 n} b_{k,i}$. Equations (5) and (6) show that the LOPV can be generated with OR and AND operations. Fig. 2 shows the circuit diagram of the NOR planes for a 64-bit merged shifter. The three NOR planes consist of an OR-AND plane for the LZC part and an additional OR plane for the shift decoder. As shown in Fig. 2, each NOR plane has pseudo-NMOS NOR gates. The largest fan-in used in the first NOR plane is a 32-bit NOR gate and the second NOR plane consists of 6-bit NOR gates. Therefore, the critical path of the first two NOR planes will include a 32-bit NOR gate, an inverter and a 6-bit NOR gate. The normalisation shifter used in this design has a two-stage shifter implemented with 16-bit and 4-bit muxes. Two decoded signals are generated by the third NOR plane, one for the 16-bit mux (from 4-bit NOR gates), and the other for the 4-bit mux (from 16-bit NOR gates).

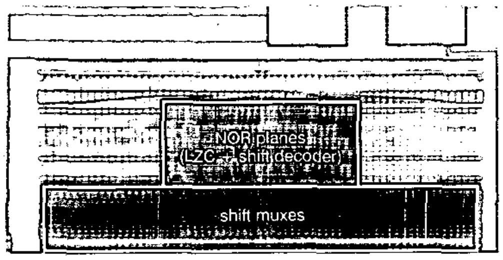

Fig. 3 *Microphotograph of fabricated chip*

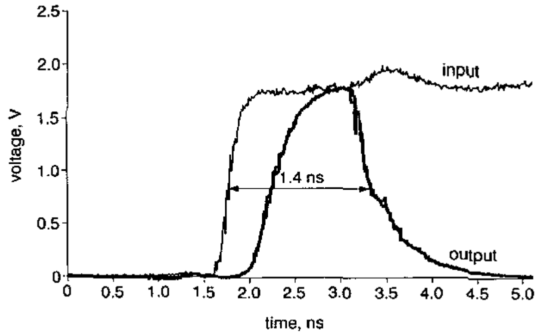

Fig. 4 *Measured delay time of fabricated chip*

Measurement result: Fig. 3 shows the microscope picture of the fabricated chip and Fig. 4 shows the measured result of the fabricated merged shifter. The waveform of the worst case vector in Fig. 4 has the glitch-like form because the latency of the shift muxes is shorter than that of the NOR planes. The total delay time of the merged shifter includes the operation time of the LZC part and the shifter. The test result shows 1.4 ns delay time for the 64-bit operand at 1.8 V power supply voltage. The power consumption of the test chip is 48 mW and the core area is 550 × 20 μm. The chip is fabricated using a five-metal 0.18 μm CMOS process.

Conclusions: A new method of floating-point normalisation has been proposed and demonstrated. The proposed normalisation scheme has a unit consisting of the LZC merged with the normalisation shifter in NOR planes. The normalisation structure generates the leading one's position value instead of a conventional shift amount value. This merged NOR-plane scheme produces shift control signals much faster than conventional LZCs with a separate shift decoder. A 64-bit normalisation operation has been executed within 1.4 ns in the fabricated normalisation unit using a 0.18 μm CMOS process at 1.8 V supply voltage.

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Low sensitivity second-order bandpass digital filter structure

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A new low sensitivity second-order bandpass digital filter structure is presented. The proposed structure has the smallest absolute angle sensitivity and a moderate radius sensitivity for the pole angle θ in the range $0.38\pi \le |\theta| \le 0.44\pi$ and $0.56\pi \le |\theta| \le 0.62\pi$ and for the radius r in the range $0.5 \le r < 1$.