

# A 2.4-GHz Sub-mW CMOS Receiver Front-End for Wireless Sensors Network

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**Abstract**—A 2.4-GHz fully integrated CMOS receiver front-end using current-reused folded-cascode circuit scheme is presented. A configuration utilizing vertically stacked low-noise amplifier (LNA) and a folded-cascode mixer is proposed to improve both conversion gain and noise figure suitable for sub-mW receiver circuits. The proposed front-end achieves a conversion gain of 31.5 dB and a noise figure of 11.8 dB at 10 MHz with 500- $\mu$ A bias current from a 1.0-V power supply. The conversion gain and noise figure improvements of the proposed front-end over a conventional merged LNA and single-balanced mixer are 11 dB and 7.2 dB at 10 MHz, respectively, with the same power consumption of 500  $\mu$ W.

**Index Terms**—Conversion gain, current-reusing, flicker noise, folded cascode, noise figure, signal-to-noise ration (SNR).

## I. INTRODUCTION

**D**UE to the rapidly growing markets of battery-operated wireless sensors network (WSN), the needs for extremely low-power single-chip wireless transceivers have drawn wide attention. These transceivers require a high level of energy efficiency to operate continuously over durations greater than one year while using only a single battery. However, a low-power transceiver design is still a challenging issue because power reduction is restricted by required system specifications such as output power, noise figure (NF), and gain. The design of a low-power implementation of RF front-end circuits is a particularly important issue. This is because the RF front-end has to be constantly turned on for waiting for a wake-up signal and its performance primarily determines the entire receiver performance of both noise figure and conversion gain.

Fig. 1 shows two conventional front-end configurations. In it are a cascaded low-noise amplifier (LNA) and mixer configuration and a merged LNA and mixer configuration. In terms of gain and of noise figure, a cascaded LNA and mixer is a better performer because the noise contribution of the mixer can be substantially suppressed by the high voltage gain of the LNA; however, its high power consumption has been a significant obstacle to its use in low-power applications. On the contrary,

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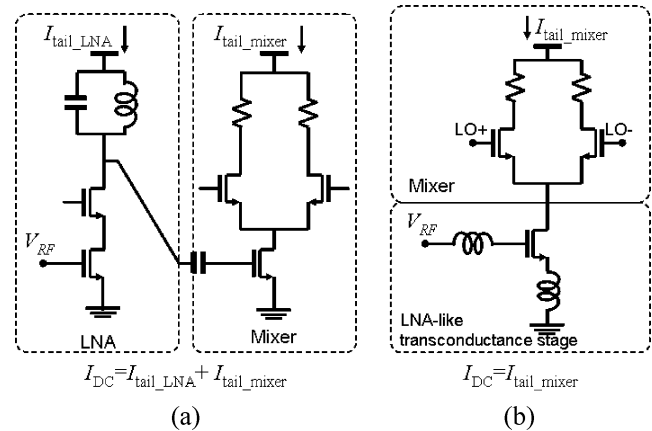


Fig. 1. Conventional front-end configurations (a) a cascaded LNA and mixer and (b) a merged LNA and single-balanced mixer.

the merged LNA and mixer scheme has been widely used in sub-mW receivers because it can reduce power consumption effectively by removing the dc current path flowing into the LNA [1], [2]. However, a problem occurs when a RF signal is directly applied to the mixer input without signal amplification in a merged LNA and mixer. This results in a low gain and a high NF which significantly hampers the entire receiver performance. In this letter, we propose a 2.4-GHz current-reused folded-cascode circuit scheme for sub-mW receiver front-end in wireless sensor network applications to achieve both high gain and low noise figures while maintaining a low power operation.

## II. CURRENT-REUSED FOLDED-CASCODE FRONT-END

Fig. 2 shows the configuration of the proposed current-reused folded-cascode receiver front-end. To prevent RF performance degradation caused by the absence of LNA, both a LNA and a mixer are implemented in the proposed front-end. In addition, in order to achieve low power consumption, we removed the dc current path from the power supply to the LNA. Instead, we have stacked a mixer above the LNA and inserted a large bypass capacitor ( $C_{bypass}$ ) between the LNA and the mixer, as this will provide a reliable ac ground. In this scheme, the LNA operates by only reusing the dc bias current of the mixer without any additional power consumption. However, if a LNA and a single-balanced (SB) mixer are vertically stacked, there may not be much voltage headroom because many transistors would be stacked between VDD to ground. In order to address this problem, we have employed a folded-cascode mixer instead of a SB mixer, as shown in Fig. 2. The local

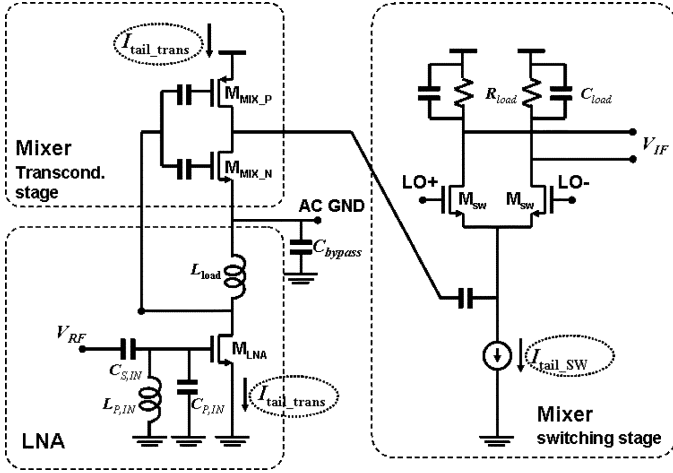


Fig. 2. Proposed current-reused folded-cascode front-end.

oscillation (LO) switching stage current of  $I_{\text{tail\_SW}}$  doesn't flow into the LNA, and the LNA only reuses the transconductance stage current of the mixer ( $I_{\text{tail\_trans}}$ ). Fortunately, the LO switching stage of the folded-cascode mixer can operate only with much lower dc current, as compared to the transconductance stage. This means that most of the dc bias current flows into the LNA so as to reuse the bias current. In addition, we have utilized an inverter-type transconductance stage instead of a conventional single nMOS transistor to enhance the gain of the mixer [3]. Therefore, we can achieve better RF performance compared to those of a cascaded LNA and mixer with this implementation of the LNA and mixer with the inverter-type transconductance stage. This uses no more than the amount of power used in the merged LNA and mixer, as it reuses the dc bias current.

### III. NOISE IMMUNITY CHARACTERISTICS

Noise figure of the proposed front-end can be substantially improved. The improvement can be explained from two points of view. First, the large voltage gain of LNA sufficiently suppresses white and flicker noises modulated by the mixer. Second, a folded-cascode mixer is intrinsically less influenced by flicker noise. In direct-conversion receivers (DCR), flicker noise is the dominant noise source since the down-converted RF signal at the mixer output is significantly corrupted by flicker noise. In the case of a low-power implementation of the mixer, it is an especially challenging issue to reduce flicker noise. In a fully symmetric differential mixer, the output signal is only affected by flicker noise generated in the switching stage [4]. In a commutating mixer, the flicker noise generated from the switching pair (MSW) slowly modulates zero-crossing points in each switching pair as shown in Fig. 3. Flicker noise makes the time of the zero-crossing of LO signals advanced by [4]

$$\Delta t = \frac{V_n(t)}{S} \quad (1)$$

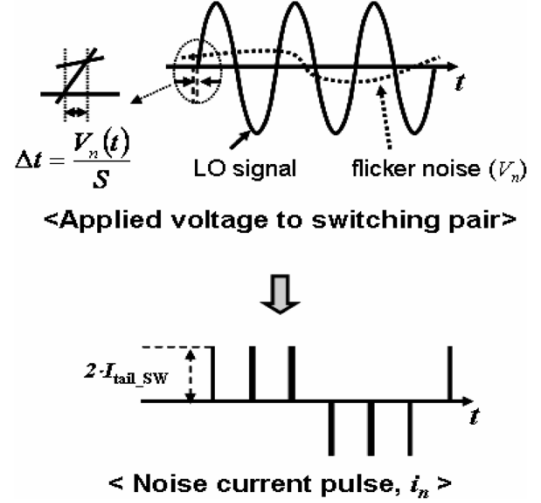


Fig. 3. Noise current generated by flicker noise at mixer output.

where  $V_n(t)$  is flicker noise voltage and  $S$  is the slope of the LO voltage at the switching time. Thus, the frequency spectrum of flicker noise at the mixer output is given by

$$i_{o,n}(f) = \frac{4I_{\text{tail\_SW}}}{T} \cdot \Delta t = I_{\text{tail\_SW}} \cdot \frac{4 \cdot V_n(f)}{S \times T} \propto I_{\text{tail\_SW}} \quad (2)$$

where  $I_{\text{tail\_SW}}$  is the dc tail current in the switching stage, and  $T$  is the period of the LO signal. This equation demonstrates that one way of lowering the mixer flicker noise is to reduce the dc current of the switching stage. Unfortunately, in a SB mixer, the bias current should be large enough to obtain a sufficient voltage gain. This is because the switching current eventually is supplied to the transconductance gain stage. However, in the proposed folded-cascode mixer, the switching current can be drastically reduced without any loss of voltage gain because the transconductance stage and the switching stage are separated in dc biasing. Therefore, the noise voltage at the mixer output caused by flicker noise is decreased by the ratio of  $I_{\text{tail\_SW\_Folded}}/I_{\text{tail\_SW\_SB}}$  compared with SB mixers, where  $I_{\text{tail\_SW\_Folded}}$  and  $I_{\text{tail\_SW\_SB}}$  are dc bias current in the switching current of the folded-cascode mixer and SB mixer, respectively.

SNR degradation caused by flicker noise can be also reduced by increasing the voltage gain in the receiver front-end. The proposed front-end can achieve  $2 \cdot (g_{m\_LNA} \cdot \omega_0 Q_{\text{load}} L_{\text{load}})$  times higher voltage gain than the conventional merged LNA and SB mixer under the assumption that nMOS and pMOS transconductances in the inverter circuit are the same. Therefore, the total SNR improvement of the proposed front-end over the merged LNA and SB mixer can be given by

$$2 \cdot (g_{m\_LNA} \cdot \omega_0 Q_{\text{load}} L_{\text{load}}) \frac{I_{\text{tail\_SW\_SB}}}{I_{\text{tail\_SW\_Folded}}}. \quad (3)$$

Equation (3) ensures that the proposed front-end will be much more immune to flicker noise as well as to white noise.

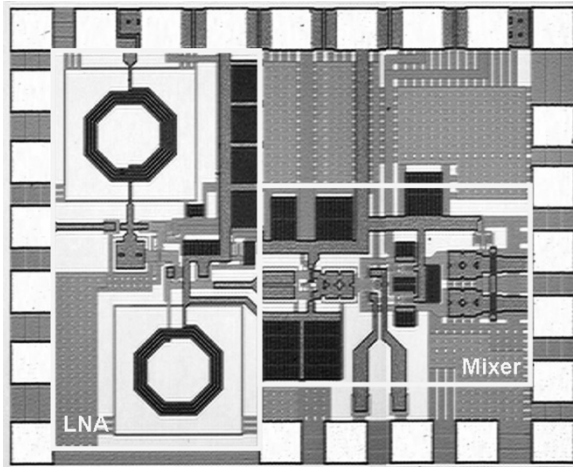


Fig. 4. Fabricated current-reused folded-cascode receiver front-end (it occupies an area of  $1.3 \text{ mm} \times 1 \text{ mm}$ ).

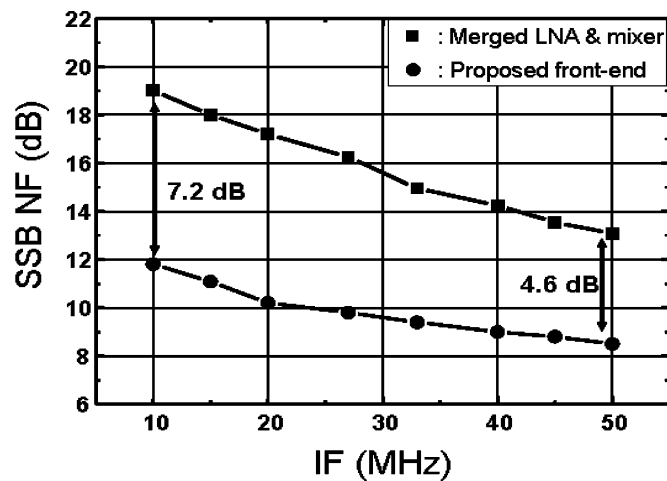


Fig. 5. Measured single-side band noise figure.

#### IV. MEASUREMENT RESULTS

Fig. 4 shows the fabricated current-reused folded-cascode front-end, which is fully integrated in  $0.18\text{-}\mu\text{m}$  1-poly six-metal CMOS technology. This chip occupies an area of  $1.3 \times 1 \text{ mm}^2$ . We also fabricated a conventional merged LNA and single-balanced mixer for performance comparisons to establish the proposed concepts. The measured conversion gain of the conventional merged LNA and SB mixer is 20.4 dB, taking only  $500 \mu\text{A}$  from a 1.0-V power supply. Additionally, in the same bias condition, the proposed current-reused folded-cascode front-end has achieved a maximum gain of 31.5 dB, which is 11-dB greater than the conventional front-end. Fig. 5 shows the measured single-side band (SSB) noise figure over the output frequency range of 10 to 50 MHz. As expected, the noise figure of the proposed front-end is at a more desirable level than that of the merged LNA and SB mixer. This is true over the entire measured frequency range. Especially notable

TABLE I  
PERFORMANCES COMPARISON [5]

	[2]	[5]	This work	This work	*Improvement
Type	Merged LNA & SB mixer	Cascaded LNA & SB mixer	Merged LNA & SB mixer	Current-reused front-end	-
Process	$0.13 \mu\text{m}$ CMOS	$0.18 \mu\text{m}$ CMOS	$0.18 \mu\text{m}$ CMOS	$0.18 \mu\text{m}$ CMOS	-
Frequency	2.35 GHz	2.44 GHz	2.4 GHz	2.4 GHz	-
Supply	1.2 V	1.8 V	1.0 V	1.0 V	-
Bias current	1.4 mA (Sim)	3.6 mA	$500 \mu\text{A}$	$500 \mu\text{A}$	-
Voltage gain	14.5 dB	21.4 dB	20.4 dB	31.5 dB	11.1 dB
NF	**24.5 dB	13.9 dB @ 2MHz	19 dB @ 10MHz	11.8 dB @ 10MHz	7.2 dB
			13.1 dB @ 50MHz	8.5 dB @ 50MHz	4.6 dB

\*Performance improvement of the proposed front-end compared with merged LNA and SB mixer in this work.

\*\*Measured from analog test output, not front-end.

is the fact that the noise figure shows a greater improvement at the lower output frequency in our graph (7.2 dB at 10 MHz and 4.6 dB at 50 MHz). This data confirms that the proposed current-reused folded-cascode front-end is much more immune to white noise as well as flicker noise due to the lower flicker noise contribution of the folded-cascode mixer and the noise screening effect of the LNA. Table I shows the summary of the measured performances of the proposed current-reused front-end compared with a fabricated conventional merged LNA and mixer and previously reported works.

#### V. CONCLUSION

We proposed and demonstrated a 2.4-GHz fully integrated CMOS receiver front-end using current-reused folded-cascode circuit scheme. The proposed front-end improves noise figure and conversion gain by employing a vertically stacked LNA and folded-cascode mixer. The fully integrated 2.4-GHz receiver front-end is fabricated using  $0.18\text{-}\mu\text{m}$  CMOS technology, and a voltage gain of 31.5 dB with a noise figure of 11.8 dB is achieved with  $500\text{-}\mu\text{W}$  power consumption.

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