

Area-efficient correlated double sampling scheme with single sampling capacitor for CMOS image sensors

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An area-efficient correlated double sampling (CDS) circuit is proposed. In conventional designs, most of the area of CDS circuits is occupied by two large on-chip sampling capacitors. A new CDS scheme is devised using only one sampling capacitor. The proposed CDS circuit has been successfully realised in a small two column pitch of 7.2 μm in a test chip fabricated using 0.18 μm CMOS process and has demonstrated fixed pattern noise less than 0.46%.

Introduction: Recently, CMOS image sensors (CISs) have been widely used because they have many advantages compared with CCD in terms of on-chip signal processing capability, low cost and low power consumption [1]. However, the image quality of CIS is poor owing to high dark current, low sensitivity and high readout noise. Among these, the readout noise problem has been a major issues in CIS. There have been many efforts to reduce readout noise using various correlated double sampling (CDS) circuits [2–5]. The CDS circuits can effectively remove fixed pattern noise (FPN), which is the dominant noise source of CIS, and they are adopted in most commercial CIS products.

However, as the number of pixels becomes higher and the size of pixel gets smaller in multi-mega pixel CISs, it is difficult to accommodate column parallel CDS circuits in a small column pitch. Typically, a CDS circuit consists of two on-chip sampling capacitors, amplifiers and several switches. Because the area of a CDS circuit is mostly occupied by two large on-chip capacitors, we need to reduce the number of sampling capacitors in order to effectively implement the circuit in a small area. In this Letter we propose an area-efficient CDS circuit scheme that requires only one sampling capacitor and four transistors. The proposed simple CDS architecture can be successfully applied for a high resolution sensor to meet recent CIS market demands.

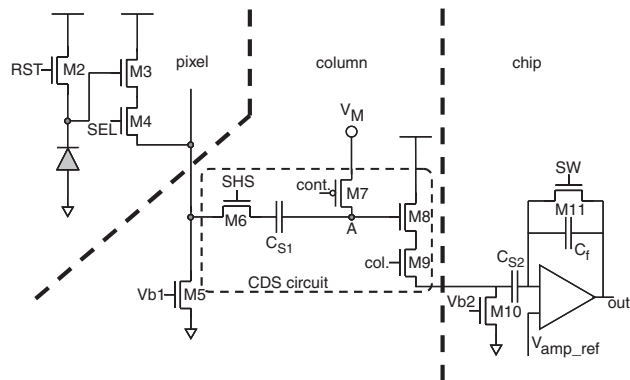


Fig. 1 Readout path of proposed CDS circuit

Proposed CDS circuit: Fig. 1 shows the readout path of the proposed CDS scheme in a prototype test CIS sensor. Because the proposed scheme is simple and uses only one capacitor, it can be compactly implemented in the two column pitch of 7.2 μm . Also, our scheme allows elimination of pixel FPN as well as column FPN. Pixel FPN is mainly caused by the mismatches of reset and source follower transistors in each pixel; on the other hand, column FPN results from mismatches of each column parallel CDS circuit. The operation timing diagram of the proposed CDS circuit is shown in Fig. 2. Pixel FPN can be removed by the double sampling technique during period 1. First, node A is connected to V_M ($= 1.5\text{ V}$) via M7, and then the signal is readout. As a result, sampling capacitor C_{S1} stores the voltage of $V_{\text{sig}} + V_{\text{pix_offset}} - V_M$. After node A is floating, the pixel reset value is readout ($V_{\text{reset}} + V_{\text{pix_offset}}$). This makes node A a voltage pixel-offset free, given by $V_A (= V_{\text{reset}} - V_{\text{sig}} + V_M)$. Column FPN can also be eliminated by the operation of a switched capacitor amplifier that is also used as an output driver. After the V_A is read (M11 is closed), V_A is reset to the reference voltage V_M again. Next, M11 is open and then the reference voltage is read. Because both readout signals, i.e. $V_A + V_{\text{col_offset}}$ and $V_M + V_{\text{col_offset}}$ include the

same column offset, the final output has an offset-free characteristic ($V_{\text{amp_ref}} + V_A \times C_{S2}/C_f$). These operations are consecutively executed column by column.

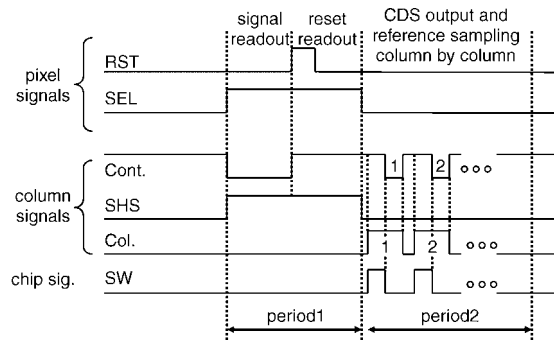


Fig. 2 Operation timing diagram of proposed CDS circuit scheme

Test sensor and measurement results: To verify the performance of the proposed CDS scheme we have designed and fabricated a prototype test sensor in CIF (352 \times 288) format using 0.18 μm 1P4M CMOS process. We have adopted a three transistor pixel with an Nwell/Psub photodiode. The size of a pixel is 3.6 \times 3.6 μm and the fill factor is 32.8%. The column parallel CDS circuits are located below the pixel array and take two column pitches in a relatively small area of 350 \times 7.2 μm . For the convenience of layout, we have placed the CDS circuit in two column pitches with a stacked two-stage CDS array. Although only one capacitor is used, more than 80% of the total area of the CDS circuit is occupied by a sampling capacitor.

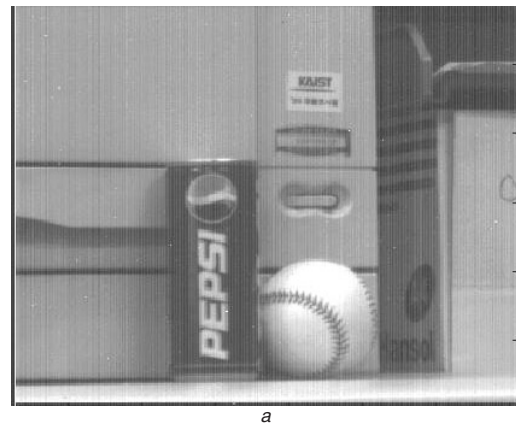


Fig. 3 Sample images from test CIS sensor

a CDS not applied
b CDS applied

Fig. 3 shows sample images with and without CDS operation. Vertical stripes caused by column FPN are easily identified in Fig. 3a. However, there is no observable column pattern for an image acquired with the proposed CDS as shown in Fig. 3b. To evaluate the FPN of the test sensor, we have measured the dark signal under no integration time condition. As shown in Fig. 4, most pixels have a value

at most within one LSB level from an average value (in 8 bit resolution) and FPN is measured to be less than 0.46%. Table 1 shows test sensor characteristics.

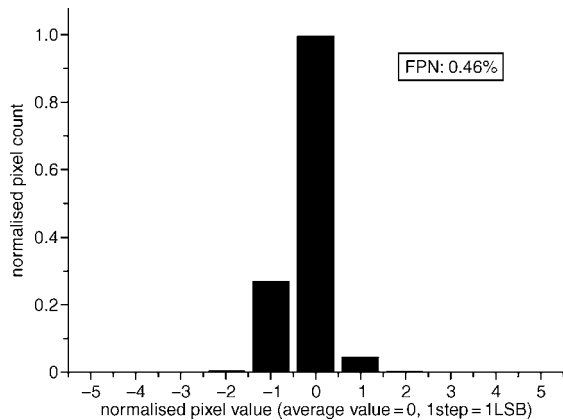


Fig. 4 Histogram of dark image under no integration time for FPN measurement

Table 1: Fabricated sensor characteristics

Process	0.18 μm 1P4M CMOS
Pixel	$3.6 \times 3.6 \mu\text{m}$, 3T
Array size	352×288
Photodiode	Nwell/Psub
Fill factor	$4.25 \mu\text{m}^2$ (32.8%)
Dark current (at 25°C)	0.48 (fA/pixel)
Saturation level	0.48 V
Conversion gain	37 ($\mu\text{V}/\text{e}^-$)
FPN (without dark)	0.46%

Conclusion: An area-efficient correlated double sampling circuit with a single sampling capacitor is proposed. The proposed CDS scheme consists of only four transistors and one sampling capacitor, to make it suitable for high resolution sensors realised in a small pixel size. We have fabricated a prototype test sensor using 0.18 μm 1P4M CMOS process and measured the sensor characteristics. The proposed scheme has been implemented in two column pitches of 7.2 μm and has achieved FPN less than 0.46%.

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